

Product data sheet

1. Product profile

1.1 General description

Passivated sensitive gate thyristor in a SOT54 plastic package.

1.2 Features

Very sensitive gate

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits

1.3 Applications

General purpose switching and phase control

1.4 Quick reference data

- $V_{DRM} \le 400 \text{ V}$
- V_{RRM} ≤ 400 V
- $I_{TSM} \le 8 \text{ A (t = 10 ms)}$

- $I_{T(RMS)} \le 0.8 A$
- $I_{T(AV)} \le 0.5 A$
- $I_{GT} \le 50 \,\mu\text{A}$

2. Pinning information

Table 1. Pinning

	_		
Pin	Description	Simplified outline	Graphic symbol
1	anode (A)		N 1
2	gate (G)		A K
3	cathode (K)	321	G sym037
		SOT54 (TO-92)	



3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BT169D-L	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Parameter	Conditions	Min	Max	Unit
repetitive peak off-state voltage		-	400	V
repetitive peak reverse voltage		-	400	V
average on-state current	half sine wave; $T_{lead} \le 83 ^{\circ}C$; see Figure 1	-	0.5	Α
RMS on-state current	all conduction angles; see Figure 4 and $\underline{5}$	-	0.8	А
non-repetitive peak on-state current	half sine wave; $T_j = 25$ °C prior to surge; see Figure 2 and 3			
	t = 10 ms	-	8	Α
	t = 8.3 ms	-	9	Α
I ² t for fusing	t _p = 10 ms	-	0.32	A ² s
rate of rise of on-state current	$I_{TM} = 2 \text{ A}; I_G = 10 \text{ mA};$ $dI_G/dt = 100 \text{ mA}/\mu\text{s}$	-	50	A/μs
peak gate current		-	1	А
peak reverse gate voltage		-	5	V
peak gate power		-	2	W
average gate power	over any 20 ms period	-	0.1	W
storage temperature		-40	+150	°C
junction temperature		-	125	°C
	repetitive peak off-state voltage repetitive peak reverse voltage average on-state current RMS on-state current non-repetitive peak on-state current I²t for fusing rate of rise of on-state current peak gate current peak reverse gate voltage peak gate power average gate power storage temperature	repetitive peak off-state voltage repetitive peak reverse voltage average on-state current half sine wave; $T_{lead} \le 83 ^{\circ}\text{C}$; see Figure 1 all conduction angles; see Figure 4 and $\frac{5}{2}$ non-repetitive peak on-state current half sine wave; $T_j = 25 ^{\circ}\text{C}$ prior to surge; see Figure 2 and $\frac{3}{2}$ the surge; see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 2 and $\frac{3}{2}$ the surge is easily see Figure 4 and $\frac{5}{2}$ in the surge is easi	repetitive peak off-state voltage repetitive peak reverse voltage average on-state current half sine wave; $T_{lead} \le 83 ^{\circ}\text{C}$; asee Figure 1 repetitive peak on-state current all conduction angles; see Figure 4 and 5 repetitive peak on-state current half sine wave; $T_j = 25 ^{\circ}\text{C}$ prior to surge; see Figure 2 and 3 repetitive peak on-state current $t = 10 \text{ms}$ repetitive of on-state current $t = 8.3 \text{ms}$ rate of rise of on-state current $t_{peak} = 10 \text{ms}$ repetitive of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak of on-state current $t_{peak} = 10 \text{ms}$ repetitive peak on-state current $t_{peak} = 10 $	repetitive peak off-state voltage - 400 repetitive peak reverse voltage - 400 average on-state current half sine wave; $T_{lead} \le 83 ^{\circ}\text{C}$; - 0.5 see Figure 1 - 0.8 and 5 - 0.8 non-repetitive peak on-state current half sine wave; $T_{j} = 25 ^{\circ}\text{C}$ prior to surge; see Figure 2 and 3 - 8 t = 8.3 ms - 9 12t for fusing to frise of on-state current $T_{j} = 10 ^{\circ}\text{ms}$ - 0.32 rate of rise of on-state current $T_{j} = 20 ^{\circ}\text{C}$ prior to surge; see Figure 2 and 3 - 9 12t for fusing to frise of on-state current $T_{j} = 20 ^{\circ}\text{C}$ prior to surge; see Figure 2 and 3 - 9 12t for fusing to frise of on-state current $T_{j} = 20 ^{\circ}\text{C}$ prior to surge; see Figure 2 and 3 - 9 12t for fusing to frise of on-state current $T_{j} = 20 ^{\circ}\text{C}$ prior to surge; see Figure 2 and 3 - 9 12t for fusing to friend the figure 2 and 3 - 9 12t for fusing to friend the figure 3 to fried

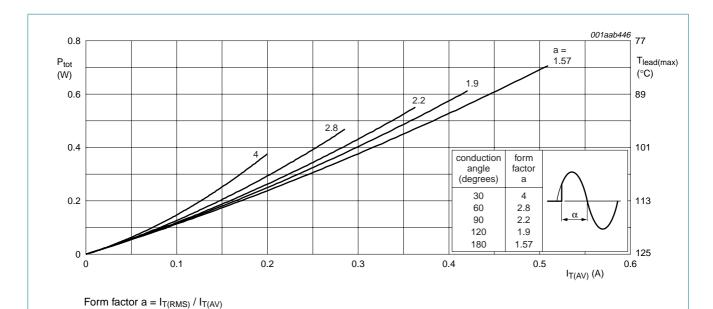
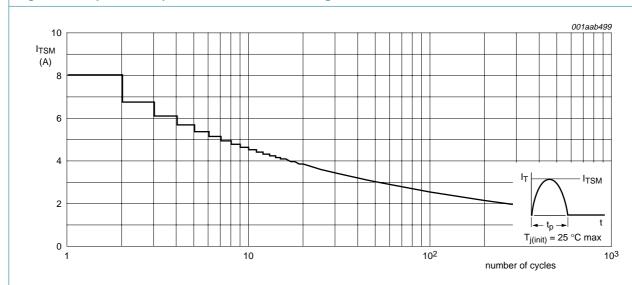


Fig 1. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

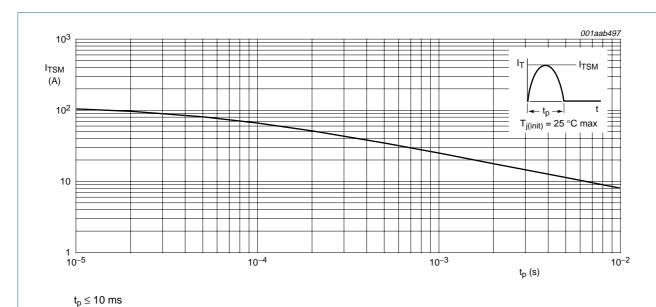


Fig 3. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

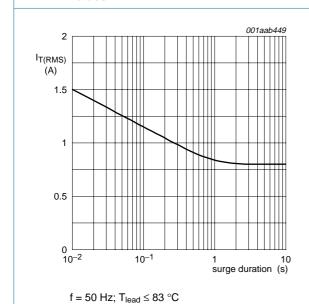
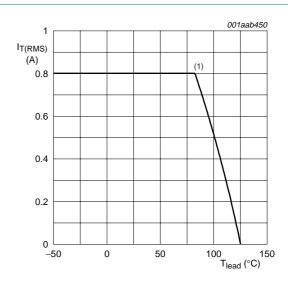


Fig 4. RMS on-state current as a function of surge duration for sinusoidal currents



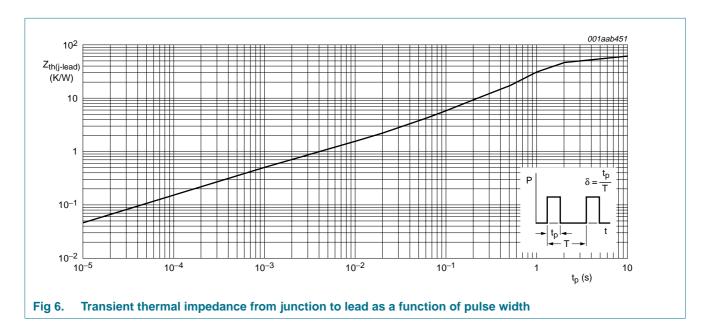
(1) $T_{lead} = 83 \, ^{\circ}C$

Fig 5. RMS on-state current as a function of lead temperature; maximum values

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j\text{-lead})}$	thermal resistance from junction to lead	see Figure 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed-circuit board mounted; lead length = 4 mm	-	150	-	K/W



6. Characteristics

Table 5. Characteristics

 $T_j = 25$ °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	racteristics					
I_{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 10 \text{ mA}; \text{ see } \frac{\text{Figure 8}}{\text{MH}}$		-	50	μΑ
lL	latching current	V_D = 12 V; I_G = 0.5 mA; R_{GK} = 1 k Ω ; see Figure 10	-	2	6	mA
I _H	holding current	V_D = 12 V; I_G = 0.5 mA; R_{GK} = 1 k Ω ; see Figure 11	-	2	5	mA
V_{T}	on-state voltage	I _T = 1.2 A	-	1.25	1.7	V
V_{GT}	gate trigger voltage	I _T = 10 mA; see <u>Figure 7</u>				
		V _D = 12 V	-	0.5	0.8	V
		$V_D = V_{DRM(max)}$; $T_j = 125 ^{\circ}C$	0.2	0.3	-	V
I _D	off-state current	$V_D = V_{DRM(max)}$; $T_j = 125$ °C; $R_{GK} = 1 \text{ k}\Omega$	-	0.05	0.1	mA
Dynamic c	haracteristics					
dV _D /dt	rate of rise of off-state voltage	$V_{DM} = 0.67 \times V_{DRM(max)}$; $T_j = 125$ °C; exponential waveform; see Figure 12				
		$R_{GK} = 1 k\Omega$	500	800	-	V/μs
		gate open circuit	-	25	-	V/μs
t _{gt}	gate-controlled turn-on time	$I_{TM} = 2 \text{ A}; V_D = V_{DRM(max)}; I_G = 10 \text{ mA}; $ $dI_G/dt = 0.1 \text{ A}/\mu\text{s}$	-	2	-	μs
t _q	commutated turn-off time	$V_{DM} = 0.67 \times V_{DRM(max)}; T_j = 125 ^{\circ}C;$ $I_{TM} = 1.6 A; V_R = 35 V;$ $(dI_T/dt)_M = 30 A/\mu s; dV_D/dt = 2 V/\mu s;$ $R_{GK} = 1 k\Omega$	-	100	-	μs

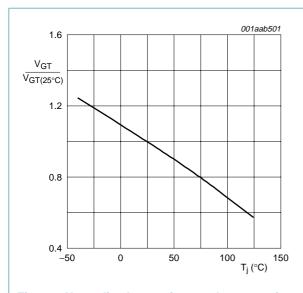


Fig 7. Normalized gate trigger voltage as a function of junction temperature

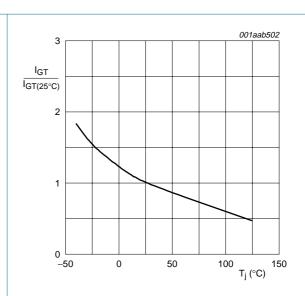
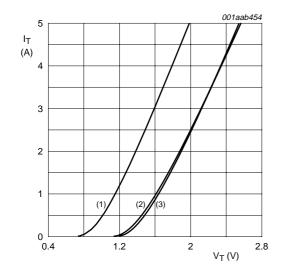


Fig 8. Normalized gate trigger current as a function of junction temperature

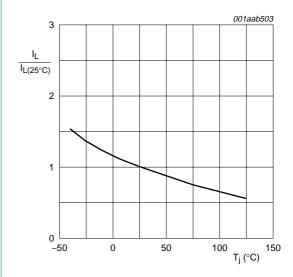


 $V_0 = 1.067 \text{ V}$

 $R_s = 0.187 \Omega$

- (1) $T_i = 125 \,^{\circ}C$; typical values
- (2) T_i = 125 °C; maximum values
- (3) $T_j = 25$ °C; maximum values

Fig 9. On-state current as a function of on-state voltage



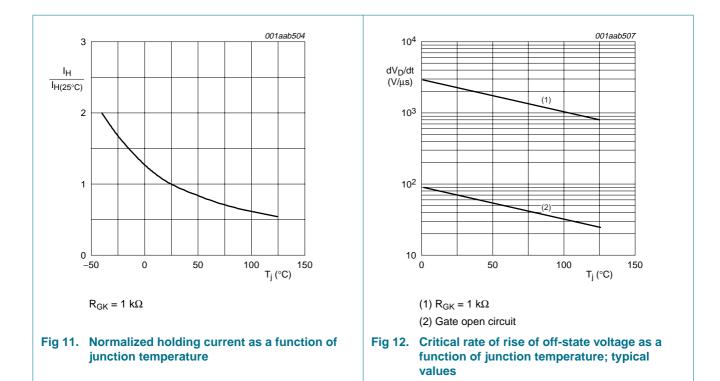
 $R_{GK} = 1 k\Omega$

Fig 10. Normalized latching current as a function of junction temperature

NXP Semiconductors BT169D-L

Thyristor logic level

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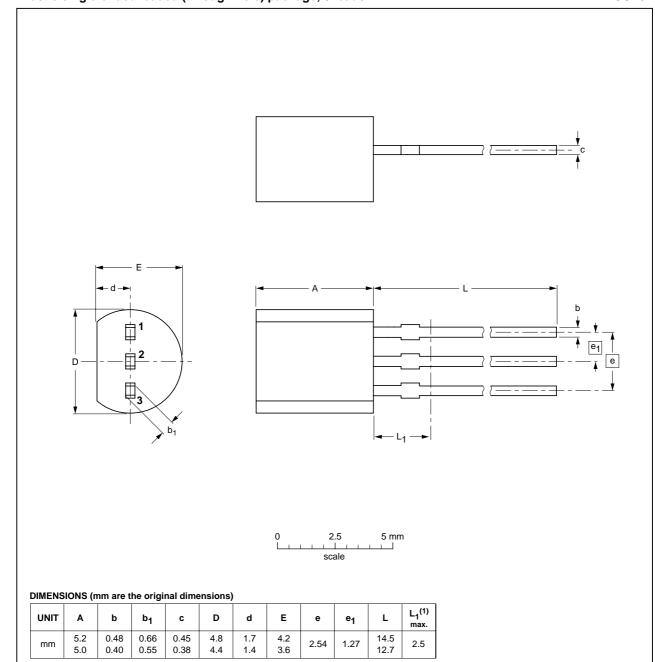
7. Package information

Epoxy meets requirements of UL 94 V-0 at 3.175 mm.

8. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE		REFER	ENCES		EUROPEAN PROJECTION ISSI	ISSUE DATE
VERSION	IEC	JEDEC	JEITA			ISSUE DATE
SOT54		TO-92	SC-43A			-04-06-28- 04-11-16

Fig 13. Package outline SOT54 (TO-92)

BT169D-L_2

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9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BT169D-L_2	20080226	Product data sheet	-	BT169D-L_1
Modifications:	 Section 1.2 "Features" on page 1: updated. Section 1.4 "Quick reference data" on page 1: condition I_{TSM} updated. Table 3 "Limiting values" on page 2: table note 1 removed. 			
		aracteristics" on page 6: condition	ns I _{GT} , I _L , I _H and V _{GT} update	ed.
BT169D-L_1	20071112	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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11. Contact information

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